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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/666,325	09/21/2000	Douglas S. Armbrust	BU9-98-110 DIV	1958

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EXAMINER

KANG, DONGHEE

ART UNIT PAPER NUMBER

2811

DATE MAILED: 06/05/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/666,325

Applicant(s)

ARMBRUST ET AL.

Examiner

Donghee Kang

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 15-34 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 15-34 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 16.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Continued Examination Under 37 CFR 1.114***

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 23 April 2002 has been entered.

### ***Information Disclosure Statement***

2. Acknowledgment is made of receipt of applicant's Information Disclosure Statement (PTO-1449) filed 22 April 2002.

### ***Claim Rejections - 35 USC § 112***

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 15, 21, & 29 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claims 15, 21, & 29 recite the limitation "said uppermost layer maintains performance of said semiconductor device irrespective of resistive shifts in lines 6, 5, 7,

respectively. The specification only discloses the invention enables less resistivity shift per percent thickness of LM layer formation.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 15, 21, & 29 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 15, 21, & 29 recite the limitation "said uppermost layer maintains performance of said semiconductor device irrespective of resistive shifts in lines 6, 5, 7, respectively. The meaning of this limitation is not clear how the uppermost layer, which is a 10 ~ 20 % of copper layer, maintains performance of said semiconductor device irrespective of resistive shifts. See response to argument.

***Claim Rejections - 35 USC § 103***

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims **15-18, 21-24, & 27-32** are rejected under 35 U.S.C. 103(a) as being unpatentable over Filipiak et al (US 5,447,887).

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Regarding claims **15-16**, Filipiak et al discloses a semiconductor device comprising (Fig.5):

a first level of silicide free copper (30); and an uppermost layer (32) of copper, wherein a top of uppermost layer comprises a silicide surface. Filipiak et al does not explicitly teach the copper layer is a bonding pad. An increase in circuit density corresponds to a decrease in conductor dimensions, which leads to higher resistances and current densities, which increase the signal losses and promote electromigration damage to the conductors on the electronic devices and packages. These problems can be solved using a copper metal because of its good electrical conductivity as known in the art. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the copper interconnect layer as a bonding pad in IC device, since the metal copper has a very good electrical conductivity.

Filipiak does not explicitly teach the uppermost layer maintains performance of semiconductor device irrespective of resistive shifts. This feature is inherent in Filipiak's device since both structures are same.

Regarding claims **17**, Filipiak et al discloses substantially the entire claimed structure, as applied to claim 15 above, except for the method of cleaning of uppermost layer by applying one of the ammonia plasma and the hydrogen plasma. This is a product-by-process limitation. "Even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production.

If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior the prior product was made by a different process". In re Thorpe, 777F. 2d 695,698 USPQ 964, 966 (Fed. Cir. 1985). See also MPEP 2113. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claim in "product by process" claim or not.

Regarding claims **18**, Filipiak et al discloses all claimed structure, as applied to claim 15 above, except for the silicide thickness which is in the range 10 % to 20 % of the total thickness of the copper interconnect layer. However, Filipiak et al mentioned the thickness of silicide can be changed depend on the application of device. See *Col.5, line 63 – Col.6, line 6*. It would have been obvious in the art at the time the invention was made to select the thickness of silicide layer, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claims **21-23, 27-31**, Filipiak et al discloses a semiconductor device comprising (Fig.5):

an exterior surface having a silicide layer; and an interior having a copper layer, wherein the silicide layer comprises a bonding pad. Filipiak et al does not teach the silicide thickness which is in the range 10 % to 20 % of the total thickness of the copper interconnect layer. However, Filipiak et al mentioned the thickness of silicide can be changed depend on the application of device. See *Col.5, line 63 – Col.6, line 6*. It would

have been obvious in the art at the time the invention was made to select the thickness of silicide layer, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Filipiak does not explicitly teach the uppermost layer maintains performance of semiconductor device irrespective of resistive shifts. However, this feature is not supported by disclosure.

Regarding claims **24 & 32**, Filipiak et al discloses all claimed structure except for the method of cleaning of uppermost layer by applying one of the ammonia plasma and the hydrogen plasma. This is a product-by-process limitation. "Even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production.

If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior the prior product was made by a different process". In re Thorpe, 777F. 2d 695,698 USPQ 964, 966 (Fed. Cir. 1985). See also MPEP 2113. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claim in "product by process" claim or not.

9. Claims **19-20, 25-26, & 33-34** are rejected under 35 U.S.C. 103(a) as being unpatentable over Filipiak et al in view of Dass et al (US 6,046,101).

Filipiak et al teaches all claimed structure, as applied to claims 15, 21, & 29 above, except for tin solder terminal electrically connected to bonding pad.

However, Dass et al teaches in Fig.21 the solder terminal (270) connected to bonding pad and a silicon nitride (245) including an opening. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the solder terminal in order to facilitate electrical connection of the semiconductor structure with an external connector, such as modulator package substrate.

### ***Response to Arguments***

10. Applicant's arguments filed August 27, 2001 have been fully considered but they are not persuasive.

The applicant argues that it has not been shown where Filipiak et al. teach or suggest the 10 % - 20 % of the copper layer is the silicide layer. These matters have been pointed out in the statement of rejection in the paragraph above with respect to claims 18, 21, & 29. Filipiak et al. teach that some applications may find benefit from siliciding the entire thickness of a copper member (**Col.6, lines 5-6**). Further, it would have been obvious in the art at the time the invention was made to select the thickness of silicide layer, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

The applicant argues that Filipaik explain the silicide layer should be less than 10 % of the metallization layer in order to avoid resistivity problems. To the contrary, the claimed invention is substantially different in that it forms the silicide to a thickness of 10



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~ 20 % without alternating performance (irrespective of resistivity shifts). However, this feature is unclear how the uppermost layer, which is a 10 ~ 20 % of copper layer, maintains performance of said semiconductor device irrespective of resistive shifts. As mentioned by applicant, Filipaik teaches a reason for limiting the thickness of the silicide layer to less than ten percent of the total copper thickness is that silicidation degrades the resistivity of the copper interconnection (See also Col.5, line 65). The same problem is expected in applicant's device because the silicide layer is more than ten percent of total copper layer. Applicant explains that this extensive silicide formation is acceptable at the last metal level...., because the last metalization layer generally comprises very thick metallurgy. However, it is noted that the features upon which applicant relies are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

### **Conclusion**

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donghee Kang whose telephone number is 703-305-9147. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Donghee Kang, Ph.D  
June 1, 2002

A handwritten signature in black ink that reads "Tom Thomas". The signature is written in a cursive style with a horizontal line above the first "T" and another horizontal line above the second "T".

**TOM THOMAS**  
**SUPERVISORY PATENT EXAMINER**  
**TECHNOLOGY CENTER 2800**